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BEFORE THE HONORABLE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 973

Application Number: 09/020,647
Filing Date: February 09, 1998
Appellants: FJELSTAD ET AL.

MAILED
SEP 11 2003
GROUP 2800

Michael J. Doherty
For Appellant

EXAMINER'S ANSWER

This is in response to appellant's brief on appeal filed 7-10-03.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

Appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is substantially correct. The changes are as follows:

In the first paragraph, change "40-41" to -- 40-42 --.

(7) Grouping of Claims

The rejection of claims 35-38, 40, 41, 43-44, 45-54 and 55-57 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand

or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,070,297	KWON et al.	12-1991
5,874,782	PALAGONIA	2-1999
4,671,849	CHEN	6-1987
4.962,985	LEGRANGE	10-1990

(10) Grounds of Rejection

In the rejections infra, reference labels are generally recited only for the first recitation of identical claim language.

The following grounds of rejection are applicable to the appealed claims:

Claims 35-38, 40-42, 45-54 and 57 stand rejected under 35 U.S.C. 102(b) as anticipated by Kwon (5070297) or, in the alternative, under 35 U.S.C. 103(a) as obvious over the combination of Kwon (5070297) and Chen (4671849).

At column 4, line 13 to column 7, line 62, Kwon teaches the following limitations of independent claims 35 and 45:

35. A method of making a compliant semiconductor chip package comprising: providing a semiconductor chip 14 having a contact bearing surface including a central region bounded by a peripheral region, wherein the peripheral region of said contact bearing surface has chip contacts 36; providing a dielectric protective layer 34 over the contact bearing surface of said semiconductor chip, said dielectric protective layer having apertures for said chip contacts; providing a compliant layer 32 over said dielectric protective layer and over the central region of the contact bearing face of said semiconductor chip, wherein said compliant layer has a substantially flat top surface, a bottom surface that is attached to said dielectric protective layer and sloping edges between the top surface and the bottom surface, wherein the sloping edges of said compliant layer have an inherent first curved transition region (illustrated but not labeled) near the top surface of said compliant layer and an inherent second curved transition region (illustrated but not labeled) near the bottom surface of said compliant layer; and selectively electroplating elongated bond ribbons 28 atop said dielectric protective layer and said compliant layer, wherein each said bond ribbon electrically connects one of said chip contacts to an associated conductive terminal 20-22-24 disposed on the top surface of said compliant

layer, and wherein said elongated bond ribbons extend along the sloping edges of said compliant layer and have a first curved region overlying the first curved transition region of said compliant layer and a second curved region overlying the second curved transition region of said compliant layer.

45. A method of making a compliant microelectronic package comprising: providing a microelectronic element 14 having a first surface and a plurality of contacts disposed on the first surface thereof; providing a compliant layer over the first surface of said microelectronic element, said compliant layer having a bottom surface facing toward said first surface of said microelectronic element, a top surface facing upwardly away from said microelectronic element and one or more sloping edge surfaces extending between the top and bottom surfaces of said compliant layer, wherein the sloping edges of said compliant layer have inherent first curved transition regions (illustrated but not labeled) near the top surface of said compliant layer and inherent second curved transition regions (illustrated but not labeled) near the bottom surface of said compliant layer; and selectively forming elongated, flexible bond ribbons over the top surface and the sloping edge surfaces of said compliant layer for electrically connecting said contacts to conductive terminals overlying the top surface of said compliant layer,

wherein said elongated, flexible bond ribbons extending along the sloping edges of said compliant layer have first curved regions overlying the first curved transition regions of said compliant layer and second curved regions overlying the second curved transition regions of said compliant layer.

Kwon also teaches, after selectively electroplating said bond ribbons, providing a second dielectric protective layer 26 over exposed elements 28 on the terminal side of said package, wherein said second dielectric protective layer has a plurality of apertures extending therethrough for providing access to said terminals, wherein said compliant layer comprises a material selected from the group consisting of silicone, flexibilized epoxy, a thermosetting polymer, fluoropolymer, thermoplastic polymer, polyimide, foams and combinations or composites thereof, providing an encapsulant layer 26 atop an exposed surface of said bond ribbons, providing a second dielectric layer 21 atop said encapsulant layer, wherein said second dielectric layer has a plurality of apertures for providing access to said terminals, wherein said dielectric layer is a silicon dioxide passivation layer provided on the contact bearing surface of said semiconductor chip, plating a barrier metal atop the contacts of said semiconductor chip, wherein said barrier metal reduces voiding at an interface between the

contacts and said bond ribbons, wherein the contacts are disposed in a first region of the first surface of said microelectronic element, and said compliant layer overlies a second region of the first surface of said microelectronic element, and wherein the sloping edges of said compliant layer extend along one or more borders between the first and second regions of the first surface of said microelectronic element, wherein said selectively forming bond ribbons step includes selectively electroplating said bond ribbons, wherein said selectively forming bond ribbons step includes depositing a conductive material over the top of said package and etching away portions of said conductive material, before the providing a compliant layer step, providing a first dielectric protective layer over the first surface of said microelectronic element, the first dielectric layer having a plurality of apertures in substantial alignment with said contacts for providing access to said contacts, the providing the compliant layer step including the step of providing the compliant layer over said first dielectric protective layer, the selectively forming flexible bond ribbons step including electroplating said bond ribbons atop said first dielectric protective layer and said compliant layer, providing a dielectric cover layer 26 over said compliant layer and said bond ribbons after the step of selectively

forming said bond ribbons, wherein said dielectric cover layer has a plurality of apertures for accessing said terminals therethrough, providing an encapsulant layer 26 over an exposed surface of said bond ribbons, providing a second dielectric protective layer 21 atop the encapsulant layer, wherein the second dielectric protective layer has a plurality of apertures for accessing said terminals therethrough, before the step of forming said bond ribbons, depositing a barrier metal 30 atop said contacts, wherein said barrier metal inherently minimizes voiding between said contacts and said bond ribbons, and wherein the sloping edge surfaces of said compliant layer extend in both vertical and horizontal directions.

To further clarify the teaching of forming elongated bond ribbons 28, it is noted that the figures of Kwon are not limited to an absolute frame of reference or otherwise limited to a particular orientation, and it is inherent that there is a frame of reference wherein the contacts 28 are small and narrow in width in proportion to length or height; therefore, the contacts are elongated.

To further clarify the teaching of inherent first transition regions near the top surface of the compliant layer and inherent second transition regions near the bottom surface of the compliant layer, it is noted that it is inherent that the

first and second regions near the top and bottom surface, respectively, transition into neighboring regions of the compliant layer and other neighboring layers.

To further clarify the teaching wherein the sloping edges of the compliant layer have a first curved transition region near the top surface of the compliant layer and a second curved transition region near the bottom surface of the compliant layer, and the elongated bond ribbons have a first curved region overlying the first curved transition region of the compliant layer and a second curved region overlying the second curved transition region of the compliant layer, it is noted that the sloping edges of the compliant layer have a first line transition region near the top surface of the compliant layer and a second line transition region near the bottom surface of the compliant layer, and the elongated bond ribbons have a first line region overlying the first transition region of the compliant layer and a second line region overlying the second transition region of the compliant layer. In addition, a line is defined by an equation so that the coordinates of its points are functions of a single independent variable or parameter; namely, the equation $y = mx + b$. Furthermore, a curved region also comprises a line defined by an equation so that the coordinates of its points are functions of a single independent variable or

parameter. Therefore, at least in this sense, the line regions of Kwon are curved.

Because applicant appears to have introduced the claim 35 limitations, "wherein the sloping edges of said compliant layer have a first curved transition region near the top surface of said compliant layer and a second curved transition region near the bottom surface of said compliant layer," and, "wherein said elongated bond ribbons . . . have a first curved region overlying the first curved transition region of said compliant layer and a second curved region overlying the second curved transition region of said compliant layer," and the claim 45 limitations, "wherein the sloping edges of said compliant layer have first curved transition regions near the top surface of said compliant layer and second curved transition regions near the bottom surface of said compliant layer," and, "wherein said elongated flexible bond ribbons . . . have first curved regions overlying the first curved transition regions of said compliant layer and second curved regions overlying the second curved transition regions of said compliant layer," primarily in order to overcome a rejection over Kwon, in the alternative, the claims are further rejected under 35 U.S.C. 103(a) as obvious over the combination of Kwon (5070297) and Chen (4671849).

Specifically, Kwon does not appear to **literally** teach curved transition regions. Nonetheless, at column 1, lines 10-13, and column 3, lines 52-64, Chen explicitly teaches curved transition regions. Moreover, it would have been obvious to combine the process of Chen with the process of Kwon because it would minimize defects in the bond ribbons.

Claim 39 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon or the combination of Kwon and Chen as applied to claims 35-38, 40-42, 45-54 and 57, and further in combination with LeGrange (4962985).

Kwon or the combination of Kwon and Chen does not appear to explicitly teach wherein the encapsulant layer material is selected from the group consisting of silicone, flexibilized epoxy, thermoplastic and gel.

Nonetheless, at column 1, lines 26-34, LeGrange teaches a process comprising a silicone encapsulation layer. In addition, it would have been obvious to combine the process of LeGrange with the process of the applied prior art because it would enable provision of the encapsulation layer of Kwon and Chen.

Claims 43, 44, 55 and 56 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon as applied to claims 35-38, 40-42, 45-54 and 57, and further in combination with Palagonia (5874782).

As cited supra, Kwon teaches, wherein the method steps are applied simultaneously to a plurality of undiced semiconductor chips 14 on a wafer 10 to form a plurality of compliant semiconductor chip packages 14, wherein the method steps are applied simultaneously to a plurality of adjacent semiconductor chips arranged in an array to form a plurality of compliant semiconductor chip packages, wherein the method is applied to a plurality of undiced semiconductor chips on a wafer to form a plurality of compliant semiconductor chip packages, and wherein the method is applied to a plurality of adjacent semiconductor chips arranged in an array to form a corresponding plurality of compliant semiconductor chip packages.

However, Kwon does not appear to explicitly teach dicing said wafer after selectively electroplating said bond ribbons to provide a plurality of individual compliant semiconductor chip packages, separating the packages after the selectively forming elongated, flexible bonds ribbons step, and separating the plurality of compliant semiconductor chip packages from one another following the step of selectively electroplating the bond ribbons.

Nevertheless, at column 1, lines 1-56; column 5, line 64 to column 6, line 6; and column 6, lines 21-39, Palagonia teaches dicing a wafer 20 after selectively electroplating bond ribbons

26 to provide a plurality of individual compliant semiconductor chip packages 22, separating packages after a selectively forming elongated, flexible bonds ribbons step, and separating the plurality of compliant semiconductor chip packages from one another following the step of selectively electroplating the bond ribbons. In addition, it would have been obvious to combine the process of Palagonia with the process of the applied prior art because it would facilitate testing of individual chips.

(11) Response to Argument

Appellant contends that Kwon does not teach "wherein elongated bond ribbons extend along the sloping edges of said compliant layer." This contention is respectfully traversed because as cited, particularly at column 5, lines 15-18, Kwon teaches that the ribbons 28 are "V-shaped," and further illustrates in Figure 2 that the V-shaped ribbons are small and narrow in width in proportion to length or height (hence elongated) along the sloping edges of compliant layer 32.

Also, applicant's argument directed to the rejection of claim 42 over the combination of prior art and Chikawa is moot because the entry of the amendment to claim 42, filed 12-09-02, unnecessitated the rejection over Chikawa.

The remaining arguments are clearly and adequately addressed in the rejections supra.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully Submitted,

David E. Graybill

Conferees:

Olik Chaudhuri

Kamand Cuneo

DEG
September 7, 2003